NASA SBIR 2022 Phase I Solicitation

Z2.02  High-Performance Space Computing Technology

Lead Center: JPL

Participating Center(s): GSFC

Scope Title

High-Performance Space Computing Technology

Scope Description

Most current NASA missions utilize 20-year-old space computing technology that is inadequate for future missions. Newer processors with improved performance are becoming available from industry but still lack the performance, power efficiency, and flexibility needed by the most demanding mission applications. The NASA High-Performance Spaceflight Computing (HPSC) project is addressing these needs. This subtopic solicits technologies that can enable future high-performance, multicore processors, along with the supporting technologies needed to fully implement avionics systems based on these processors.

- Fault-tolerant internet protocol (IP) core supporting Ethernet, Time-Sensitive Networking (TSN), Time-Triggered Ethernet (TTE), and remote direct memory access (RDMA) over converged Ethernet (RoCE) to support processor clustering.
- Compilers that support software-implemented fault tolerance (SIFT) capabilities (e.g., control flow checking, coordinated checkpoint/rollback, recovery block) for multicore processors are desired.
  - Compile-time fault tolerance is desired by NASA for reorganizing execution code to automatically build redundancy in stall cycles without requiring additional development from the user; this would be exceptional for performance optimization of code without putting additional burden on the developers. This is increasingly important with the adoption of more complex and commercial processors in future missions.
- Radiation-tolerant, point-of-load (POL) converters that feature multiple outputs, intelligent communication, or high power.
  - Modern and next-generation processors require multiple voltage supply levels, requiring multiple discrete POL converters occupying valuable processor card real estate. A multiple-output POL would enable smaller and more powerful spaceflight processing platforms.
  - Future spaceflight systems have increased needs for fault detection, tolerance, and command ability. A POL converter capable of communicating with command-and-control architectures to report health status, telemetry, or to adjust parameters is desired.
  - Future high-powered spaceflight processing applications will have a need for high-power POL converters. Specifically, converters capable of providing low voltage, but high currents (tens of amps) are desired.
- Coprocessors to (a) accelerate onboard artificial intelligence applications, or (b) perform digital signal processing (DSP) functions. Specifically, technologies are sought that either enable the reliable use of...
commercial off-the-shelf (COTS) coprocessors in space systems, or fault-tolerant IP cores that can be implemented in a radiation-hardened field-programmable gate array (FPGA).

- Radiation-tolerant solid-state memory drives (minimum 1-TB capacity) with Peripheral Component Interconnect Express (PCIe) interface, supporting file systems with industry-standard Non-Volatile Memory Express (NVMe) software stack.
- Checkpointing and recovery mechanism for single-process flight software applications.
  - Especially with increased use of COTS processors, single-event functional interrupts (SEFIs) have a high chance the processor will need to reset or incur a kernel panic. NASA desires a way for the flight software to be automatically checkpointed or have some sort of functional save-state to recover before the upset.
  - Current methodologies for resetting and recovering processors and flight software applications can incur considerable downtime and data loss. A more intelligent, rapid method for resetting and recovering is desired. NASA's Core Flight Software (cFS) would be an ideal candidate software to implement this capability.

Expected TRL or TRL Range at completion of the Project

1 to 4

Primary Technology Taxonomy

Level 1

TX 02 Flight Computing and Avionics

Level 2

TX 02.X Other Flight Computing and Avionics

Desired Deliverables of Phase I and Phase II

- Analysis
- Prototype
- Hardware
- Software
- Research

Desired Deliverables Description

Phase I Deliverables:

For software and hardware elements, a solid conceptual design, plan for full-scale prototyping, and simulations and testing results to justify prototyping approach. Detailed specifications for intended Phase II deliverables.

Phase II Deliverables:

For software and hardware elements, a prototype that demonstrates sufficient performance and capability and is ready for future development and commercialization.

State of the Art and Critical Gaps

Most NASA missions utilize processors with in-space-qualifiable high-performance computing that has high power dissipation (approximately 18 W), and the current state-of-practice Technology Readiness Level 9 (TRL-9) space computing solutions have relatively low performance (between 2 and 200 DMIPS (Dhrystone million instructions per second) at 100 MHz). A recently developed radiation-hardened processor provides 5.6 GOPS (giga operations per second) performance with a power dissipation of 17 W. Neither of these systems provides the desired performance, power-to-performance ratio, or flexibility in configuration, performance, power management, fault tolerance, or extensibility with respect to heterogeneous processor elements. Onboard network standards exist that...
can provide >10 Gbps bandwidth, but not everything is available to fully implement them.

**Relevance / Science Traceability**

The high-performance spaceflight computing (HPSC) ecosystem is enhancing to most major programs in the Human Exploration and Operations Mission Directorate (HEOMD). It is also enabling for key Space Technology Mission Directorate (STMD) technologies that are needed by HEOMD, including the Safe and Precise Landing - Integrated Capabilities Evolution (SPLICE) project. Within the Science Mission Directorate (SMD), strong mission pull exists to enable onboard autonomy across Earth science, astrophysics, heliophysics, and planetary science missions. There is also relevance to other high-bandwidth processing applications within SMD, including adaptive optics for astrophysics missions and science data reduction for hyperspectral Earth science missions.

**References**