NASA SBIR 2019 Phase I Solicitation

Z6.01 High Performance Space Computing Technology

Lead Center: JPL

Participating Center(s): GSFC

Technology Area: TA11 Modeling, Simulation, Information Technology and Processing

The NASA state-of-the-art in space computing utilizes 20-year-old technology and is inadequate for future missions. In conjunction with the US Air Force, NASA is investing in the development of the High Performance Space Computing (HPSC) Chiplet, a radiation-hardened multi-core processor that will improve space computing capabilities by two orders of magnitude. While these efforts will provide an underlying platform, they do not provide the full range of advanced computing capabilities and programming support that developers will require to support missions currently in the planning stage for the mid-2020s and beyond. Topics of interest include:

- *Fault Tolerant, Real Time Linux* - a flight qualifiable version of Linux for the HPSC Chiplet, capable of supporting parallel and heterogeneous processing for autonomy, robotics and science codes is desired. Initial design of a verifiably reliable, fault tolerant, real time Linux kernel is desired. A successful development will potentially result in an eventual Phase 3 award, or alternate funding, to develop a complete, qualified, operating system.
- *HPSC Chiplet Hypervisor* - a bare metal hypervisor capable of supporting symmetric and asymmetric multi-processing, as well as high levels of fault tolerance is desired.
- *Network Switches/Routers* - rad hard, low power switches and routers that support system level fault tolerance and testability are required for sRIO (3.1, 4.0, and above).
- *Neuromorphic computing and Machine Learning* - general purpose neural networks and other machine learning accelerators for robotic vision, system health management and similar applications are needed to meet performance power requirements in future autonomous robotic systems. Initial design of this ASIC and a validated FPGA implementation of critical portions of the design is desired. A successful development will potentially result in an eventual Phase 3 award, or alternate funding, to implement the final chiplet.
- *Graphics Processing* - low power, high performance GPU capability to support crewed vehicle displays, including virtual and augmented reality hardware is desired. An initial GPU chiplet design with validated FPGA implementation of critical portions of the design is desired. A successful development will potentially result in an eventual Phase 3 award, or alternate funding, to implement the final chiplet.

An HPSC ecosystem is of interest to all major programs in Human Exploration & Operations Mission Directorate (HEOMD) and Science Mission Directorate (SMD). Immediate infusion targets include Mars Fetch Rover, WFIRST/Chronograph, Gateway, SPLICE/Lunar Lander. Desired deliverables with regards to hardware elements include a preliminary detailed design ready for fabrication and productization.

The expected Technology Readiness Level (TRL) range at completion of this project is 4 to 6.

NASA has plans to purchase services for delivery of payloads to the Moon through the Commercial Lunar Payload

Services (CLPS) contract. Under this subtopic, proposals may include efforts to develop payloads for flight demonstration of relevant technologies in the lunar environment. The CLPS payload accommodations are yet to be precisely defined, however at least for early missions, proposed payloads should not exceed 15 kilograms in mass and not require more than 8 watts of continuous power. Smaller, simpler, and more self-sufficient payloads are more likely to be accommodated. Commercial payload delivery services may begin as early as 2020 and flight opportunities are expected to continue well into the future. In future years it is expected that payloads of higher mass and with higher power requirements might be accommodated. Selection for award under this solicitation will not guarantee selection for a lunar flight opportunity.

References:

- https://www.nasa.gov/press-release/goddard/2017/nasa-selects-high-performance-spaceflight-computing-hpsc-processor-contractor